REMARKS/ARGUMENTS

In this amendment, claim 19 is amended to add a period to the end of the claim. No claims are added or canceled. No new matter is added. Thus, claims 1-32 remain pending.

Claim Rejections 35 USC § 103(a), Narita in view of Yu

Claims 1-6, 11-19, 24-27, and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narita et al. (hereafter Narita)(US Pat. 5,293,558) in view of Yu et al. (hereafter Yu)(US Pat. 6,523,055).

Claims 1-13

Claim 1 is allowable over the above references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1. For example, claim 1 recites:

> *A multiplication unit comprising a 2N-bit multiplier and having a first short word length multiplication mode and a second long word length multiplication mode, wherein a short word length is N and a long word length is 2N, wherein N is an integer, and wherein:*
>
> *in the first mode for multiplying two N-bit numbers, a first long word length multiplicand is formed from a first short word length multiplicand, a second long word length multiplicand is formed from a second short word length multiplicand, and the first and second long word length multiplicands are multiplied together using the 2N-bit multiplier to form a result which includes the product of the first and second short word length multiplicands, and*
>
> *in the second mode for multiplying two 2N-bit numbers, wherein a third long word length multiplicand is formed from a first pair of short word length words and a fourth long word length multiplicand is formed from a second pair of short word length words, first words of the first and second pairs of short word length words are stored in respective registers connected to the 2N-bit multiplier, and subsequently the third and fourth long word length multiplicands are multiplied together using the 2N-bit multiplier.*

At page 3, the Office Action asserts that Narita uses a 2n-bit multiplier 10 in multiplying an n-bit number X and an n-bit number Y to obtain a 2n-bit result. *See Narita*, FIGS. 1-3 and col. 4 lines 29-63. However, a 2n-bit multiplier would output a 4n-bit result, not a 2n-bit result. Thus, the multiplier 10 is an n-bit multiplier producing the 2n-bit result. This interpretation is confirmed by the bus 14, which receives the output from multiplier 10, being

2n-bits. *Id.*, col. 4 lines 53-56. Also Narita makes no mention of a 2n-bit multiplier in this cited section or where the other 2n-bit part of the 4n-bit result would be output. Accordingly, Narita does not teach or suggest "*using the 2N-bit multiplier*" in "*multiplying two N-bit numbers,*" as recited in claim 1.

Additionally, the multiplication of a 2n-bit number X and a 2n-bit number Y is performed using the n-bit multiplier 10. Although FIG. 10 appears to show the multiplier 10 multiplying a 2n-bit number by a 2n-bit number, FIGS. 11 and 12 and their accompanying text describe how multiplier 10 is actually used to multiply n-bit sections of 2n-bit numbers.

For example, to multiply a 2n-bit number X and a 2n-bit number Y, the numbers X and Y are broken up into n-bit constituent parts X_H, X_L and Y_H,Y_L respectively. *Id.*, FIG. 12 and col. 10 lines 44-48. The MULT 10 multiplies the 4 combinations of the respective n-bit parts, which are in MSR 12 and MSR 13, and outputs the partial results on the 2n-bit bus 14. *Id.*, col. 9 lines 49-61. The partial products (X_H x Y_H), (X_H x Y_L), (X_L x Y_H), (X_L x Y_L) are then added to form the 4n-bit result. *Id.*, FIG. 12 and col. 10 lines 49-51. Thus, Narita uses the n-bit multiplier 10 four times to obtain 4 partial products that are added together as part of a 2n-bit by 2n-bit multiplication. In contrast, claim 1 recites that the first mode multiplies two 2N-bit number "*using the 2N-bit multiplier.*"

Regarding Yu, Yu teaches that results of a multiplication may need to be aligned before adding, which is done by a shifting circuit 130. *See Yu*, FIGS. 1B and 1C and col. 6 line 54- to col. 7 line 7. This teaching simply corresponds to the digit matching of Narita that is performed for the partial sums. *See Narita*, FIG. 12 and col. 10 lines 51-55. Thus, the combination would be the same as Narita. Also, this shifting is performed on results and not multiplicands (state before the multiplication), as recited in claim 1. Therefore, the combination of Yu with Narita does not make up for the above deficiencies in Yu.

For at least the reasons stated above, Applicant submits that claim 1 and its dependent claims 2-13 are allowable over the cited references.

Claims 14-32

Applicants submit that independent claims 14 and 26 should be allowable for at least this same rationale. Claims 15-25 depend from claim 14; and claims 27-32 depend from claim 26 and thus derive patentability at least therefrom.

Other rejections under 35 U.S.C. § 103(a)

Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narita in view of Yu as applied to claims 6 and 19 above, and further in view of Henderson et al. (hereafter Henderson)(US Pat. 6,484,194).

Claims 8-10, 21-23, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narita in view of Yu as applied to claims 1, 14, and 26 above, and further in view of Bosshart (US Pat. 4,754,421).

These claims derive patentability from their respective independent claims, which area allowable described above. The cited teachings of Henderson and Bosshart fail to make up for the deficiencies in Narita and Yu.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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